CLAIMS

What is claimed is:

1. An apparatus comprising:

a first memory having KN locations to store K sums of mixer samples during an epoch interval, the mixer samples being generated at a first clock frequency from a mixer for N channels corresponding to N satellites in a global positioning system (GPS) receiver;

an address counter coupled to the first memory to generate an address modulo-KN corresponding to a first location in the memory at the first clock frequency; and

an adder coupled to the mixer and the first memory to add one of the mixer samples to contents of the first location to generate a sum, the sum being written into the first location.

2. The apparatus of claim 1 further comprising:

a second memory coupled to the first memory and the address counter to store the K sums of mixer samples transferred from the first memory at end of the epoch interval.

3. The apparatus of claim 1 further comprising:

an epoch control circuit to generate an epoch signal indicative of the epoch interval.

4. The apparatus of claim 3 wherein the epoch control circuit comprises:

N epoch interval generators to generate N channel interval signals;

a decoder to enable one of the N epoch interval generators; and

a multiplexer coupled to the N epoch interval generators to select one of the N channel interval signals, the selected one of the N channel interval signals corresponding to the epoch signal.

5. The apparatus of claim 1 wherein K = 22 and N = 12.

6. The apparatus of claim 5 wherein the first clock frequency is equal to twenty-four times a coarse/acquisition chip rate of the GPS receiver.

7. An apparatus comprising:

a mixer circuit to mix a de-spreaded sample with coefficients to generate a mixer sample at a first clock frequency, the de-spread sample being provided by a de-spreader circuit for a signal received from one of N satellites in a global positioning system (GPS);

a look-up table coupled to the mixer circuit to generate the coefficients based on a carrier numerically controlled oscillator (NCO) value; and

a carrier NCO coupled to the look-up table to generate a carrier NCO value.

8. The apparatus of claim 7 wherein the de-spread sample includes de-spread in-phase and de-spread quadrature components, each component having 6 bits.

9. The apparatus of claim 8 wherein the coefficients include a sine and cosine values, each value having three bits.

10. The apparatus of claim 9 wherein the mixer sample includes mixer in-phase and quadrature components.

11. The apparatus of claim 9 wherein the mixer circuit comprises:

an in-phase circuit to generate the mixer in-phase component based on a first complex multiplication on the de-spread in-phase and quadrature components and the sine and cosine values, the mixer in-phase component having 8 bits; and

a quadrature circuit to generate the mixer quadrature component based on a second complex multiplication on the de-spread in-phase and quadrature components and the sine and cosine values, the mixer quadrature component having 8 bits.

12. The apparatus of claim 7 wherein the carrier NCO comprises:

N carrier base circuits to generate N carrier channel NCO values at a second clock frequency, each of the N carrier base circuits having an increment register to store an increment value loaded from a processor;

a decoder coupled to the N carrier base circuits to enable loading of one of the N increment registers based on a channel select value; and

a multiplexer coupled to the N carrier base circuits to select the carrier NCO value from the N carrier channel NCO values at the first clock frequency.

13. The apparatus of claim 11 wherein N = 12.

14. The apparatus of claim 12 wherein the first clock frequency is equal to twenty-four times a coarse/acquisition chip rate of the GPS.

15. The apparatus of claim 13 wherein the second clock frequency is equal to one-quarter times a coarse/acquisition chip rate of the GPS.

16. A method comprising:

storing K sums of mixer samples during an epoch interval, the mixer samples being generated at a first clock frequency from a mixer for N channels corresponding to N satellites in a global positioning system (GPS) receiver;

generating an address modulo-KN corresponding to a first location in the memory at the first clock frequency; and

adding one of the mixer samples to contents of the first location, the sum being written into the first location.

17. The method of claim 16 further comprising:

storing the K sums of mixer samples transferred from the first memory at end of the epoch interval.

18. The method of claim 16 further comprising:

generating an epoch signal indicative of the epoch interval.

19. The method of claim 18 wherein the epoch control circuit comprises:

generating N channel interval signals;

enabling one of the N epoch interval generators; and

selecting one of the N channel interval signals, the selected one of the N channel interval signals corresponding to the epoch signal.

20. The method of claim 16 wherein K = 22 and N = 12.

21. The method of claim 20 wherein the first clock frequency is equal to twenty-four times a coarse/acquisition chip rate of the GPS receiver.

22. A method comprising:

mixing a de-spreaded sample with coefficients to generate a mixer sample at a first clock frequency, the de-spread sample being provided by a de-spreader circuit for a signal received from one of N satellites in a global positioning system (GPS);

generating the coefficients based on a carrier numerically controlled oscillator (NCO) value; and

generating a carrier NCO value.

23. The method of claim 22 wherein the de-spread sample includes de-spread in-phase and de-spread quadrature components, each component having 6 bits.

24. The method of claim 23 wherein the coefficients include a sine and cosine values, each value having three bits.

25. The method of claim 24 wherein the mixer sample includes mixer in-phase and quadrature components.

26. The method of claim 24 wherein the mixer circuit comprises:

generating the mixer in-phase component based on a first complex multiplication on the de-spread in-phase and quadrature components and the sine and cosine values, the mixer in-phase component having 8 bits; and

generating the mixer quadrature component based on a second complex multiplication on the de-spread in-phase and quadrature components and the sine and cosine values, the mixer quadrature component having 8 bits.

27. The method of claim 22 wherein the carrier NCO comprises:

generating N carrier channel NCO values at a second clock frequency, each of the N carrier base circuits having an increment register to store an increment value loaded from a processor;

enabling loading of one of the N increment registers based on a channel select value; and

selecting the carrier NCO value from the N carrier channel NCO values at the first clock frequency.

28. The method of claim 26 wherein N = 12.

29. The method of claim 27 wherein the first clock frequency is equal to twenty-four times a coarse/acquisition chip rate of the GPS.

30. The method of claim 28 wherein the second clock frequency is equal to one-quarter times a coarse/acquisition chip rate of the GPS.

31. A receiver comprising:

a mixer circuit to mix de-spreaded samples with coefficients to generate mixer samples at a first clock frequency, the de-spread samples being provided by a de-spreader circuit for a signal received from one of N channels corresponding to N satellites in a global positioning system (GPS);

a carrier numerically controlled oscillator (NCO) circuit coupled to the mixer to generate the coefficients based one of the N channels, the NCO circuit comprising:

a first memory having KN locations to store K sums of the mixer samples during an epoch interval,

an address counter coupled to the first memory to generate an address modulo-KN corresponding to a first location in the first memory at the first clock frequency, and

an adder coupled to the mixer and the first memory to add one of the mixer samples to contents of the first location, the sum being written into the first location.

32. The receiver of claim 31 further comprising:

a second memory coupled to the first memory and the address counter to store the K sums of mixer samples transferred from the first memory at end of the epoch interval.

33. The receiver of claim 31 further comprising:

an epoch control circuit to generate an epoch signal indicative of the epoch interval.

34. The receiver of claim 33 wherein the epoch control circuit comprises:

N epoch interval generators to generate N channel interval signals;

a decoder to enable one of the N epoch interval generators; and

a multiplexer coupled to the N epoch interval generators to select one of the N channel interval signals, the selected one of the N channel interval signals corresponding to the epoch signal.

35. The receiver of claim 31 wherein K = 22 and N = 12.

36. The receiver of claim 35 wherein the first clock frequency is equal to twenty-four times a coarse/acquisition chip rate of the GPS receiver.

37. A receiver comprising:

a de-spread circuit to de-spread a sample for a signal received from one of N satellites in a global positioning system (GPS); and

a Doppler circuit coupled to the de-spread circuit to remove Doppler frequency, the Doppler circuit comprising:

a mixer circuit to mix the de-spreaded sample with coefficients to generate a mixer sample at a first clock frequency;

a look-up table coupled to the mixer circuit to generate the coefficients based on a carrier numerically controlled oscillator (NCO) value; and

a carrier NCO coupled to the look-up table to generate a carrier NCO value.

38. The receiver of claim 37 wherein the de-spread sample includes de-spread in-phase and de-spread quadrature components, each component having 6 bits.

39. The receiver of claim 38 wherein the coefficients include a sine and cosine values, each value having three bits.

40. The receiver of claim 39 wherein the mixer sample includes mixer in-phase and quadrature components.

41. The receiver of claim 39 wherein the mixer circuit comprises:

an in-phase circuit to generate the mixer in-phase component based on a first complex multiplication on the de-spread in-phase and quadrature components and the sine and cosine values, the mixer in-phase component having 8 bits; and

a quadrature circuit to generate the mixer quadrature component based on a second complex multiplication on the de-spread in-phase and quadrature components and the sine and cosine values, the mixer quadrature component having 8 bits.

42. The receiver of claim 37 wherein the carrier NCO comprises:

N carrier base circuits to generate N carrier channel NCO values at a second clock frequency, each of the N carrier base circuits having an increment register to store an increment value loaded from a processor;

a decoder coupled to the N carrier base circuits to enable loading of one of the N increment registers based on a channel select value; and

a multiplexer coupled to the N carrier base circuits to select the carrier NCO value from the N carrier channel NCO values at the first clock frequency.

43. The receiver of claim 41 wherein N = 12.

44. The receiver of claim 42 wherein the first clock frequency is equal to twenty-four times a coarse/acquisition chip rate of the GPS.

45. The receiver of claim 43 wherein the second clock frequency is equal to one-quarter times a coarse/acquisition chip rate of the GPS.